Remarks

Claims 1-15 are pending in the above-identified application. Claims 1, 4, 7, 10, 12, and 13 are amended, and claims 2-3, 5, 6, 8, 9, 11, 14 and 15 are original.

The Examiner rejected claims 1 - 15 under 35 U.S.C. 102(e) as being anticipated by Paajanin et al. (US Patent 7,349,404).

The following legal requirement is quoted from MPEP 2131 and establishes what is required to sustain a rejection under 35 U.S.C. §102. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Paajanin et al. discloses a method and system for connection set-up in a communication system which comprises a plurality of first processing units, e.g. switching units, and a plurality of second processing units, and transmits information as a stream of information cells having cell identification. For reducing the number of messages in setting up connections, the first processing units are connected to the second processing units, and information cells are supplied to several processing units, which distinguish between the cells based on the cell identification for further processing. The information is preferably ATM transmitted, and all first processing units are connected to all second processing units using virtual path connections on the ATM layer. The processing unit to which the information cell is directed is identified using virtual channel.

Regarding FIG. 1, Paajanin et al. teach as follows:

"FIG. 1 illustrates the resulting topology structure with fully developed virtual path connections 2 between the AAL switching units 1 and the DSP (Digital Signal Processor) units 3. The virtual path connections are generated not only between all switching units 1 and all DSP units 3 but also between each of the switching units 1 as shown in FIG. 1."

When the VPC (Virtual Path Connection) topology shown in FIG. 1 is created beforehand, the number of ATM-layer level connection setups and deletions are reduced during runtime to zero.

The basic solution to use VPCs on the ATM layer is no problem for the hardware. Likewise, the VC (Virtual Channel) reservation is not problematic for the hardware.

DSP units (e.g. Cofigurable DSPs) 2 and AAL2 Units 1 are, in this embodiment, units with several processors. Each processor is capable of receiving and sending cells (i.e. processors have SAR capabilities). There is preferably only one interface for each unit which is shared (commonly used) by each processor of the respective unit. In such an environment a capability to transfer a cell (information or message cell) through one interface to the appropriate processor is needed. Furthermore, the functionality of sharing this interface between several processors sending at the same time is necessary.

The hardware part of the present invention provides both these functionalities and comprises a FIFO memory 4 (FIG. 2) which may consist of an UTOPIA extender and/or a First-In First-Out buffer. Regarding the specification of UTOPIA, see for instance TR 100 815 V1.1.1 (1999-02) of ETSI (European Telecommunications Standards Institute), or AF-PHY-0017.000: "The ATM Forum Technical Committee, UTOPIA Specification, Level 1, Version 2.01"."

In Paajanin et al. a virtual path (VP) means a unidirectional transport of ATM cells that are associated by a common identifier value. A virtual path connection (VPC) is a concatenation of virtual path links that extends between the point where the virtual channel identifier values are assigned and the point where those virtual values are translated or removed.

In Paajanin et al. the invention provides a virtual path piping (in the following also termed VP-piping) which is a simple and yet very effective concept which significantly increases the performance by reducing the amount of required messages in the connection setup. This concept utilizes only the basic ATM functionalities and makes advantage of the hardware concept used in the system.

In Paajanin et al. the key idea of the VP piping is to connect all the switching units in the adaptation layer such as AAL (e.g. AAL2) switching units, to all processing units such as DSP processing units, with virtual path connections (VPC). This leads to the creation of a full mesh topology between the AAL (e.g. AAL2) and DSP units.

Paajanin et al. also teach the following: "In the new VP-piping concept presented here, the set-up uses a co-operation between DSP RM (Resource Manager) and AAL2 connection control. This co-operation means that both resource managers select a set of resources (AAL2 switching unit and DSP processors) where there is still resources available for a new "connection". The term "set of resources" means the exact processor/DSP processor that is available for the leg. The processor further defines a set of VPC connections. A set of VPC connections are all the connections from one unit (as already stated above, unit's processors share the VPC). The set of VPCs might be limited below maximum if CAC (Connection Admission Control) functionality considers certain VPC as fully booked. The sets defined by both resource

managers involved (DSP RM-AAL2 CC (connection control), or AAL2 CC and AAL2 CC) is compared with each other--the comparison result indicates the set of possible VPCs to be used for this leg and one of those is selected. These procedures are the basic rules. Additionally, for example, the macro diversity combining function can further restrict the selection DSP unit to exactly one possible unit since the unit already handles one "sister" leg of same connection. The selection of the AAL2 switching unit may also be restricted to one unit if that unit handles the N_cid required. In these case the set is actually limited to only these sets of VP connections that are possible. In some case there is only VPC possible. If it does not have resource available, the connection needs to be rejected."

Each of the independent claims of the present application have been amended to distinguish the claims over the prior art. In particular, the following feature has been included in each of the independent claims: a substantially even distribution of calls among the transcoders is established for an uneven call load on the external PVCs.

This feature is not disclosed or taught by Paajanin et al.

Since the dependent claims include all the limitations of the respective independent claims upon which they depend, the dependent claims are therefore also allowable over the cited prior art for the reasons set forth above with respect to the independent claims.

Applicants respectfully submit that the applied references, taken singly or in combination, assuming, arguendo, that the combination of the applied references is proper, do not teach or suggest one or more elements of the claimed invention. Applicants have discussed herein one or more differences between the cited prior art, and the claimed invention with reference to one or

more parts of the cited prior art. This discussion, however, is in no way meant to acquiesce in any characterization that one or more parts of cited prior art correspond to the claimed invention.

Reconsideration and withdrawal of the rejections is therefore respectfully requested. In view of the above remarks, allowance of all claims pending is respectfully requested.

This application is believed to be in condition for allowance, and such action at an early date is earnestly solicited. If a telephone conference would be of assistance in advancing the prosecution of this application, the Examiner is invited to call applicant's attorney.

Respectfully submitted,

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